REMARKS

This is a full and timely response to the outstanding final Office Action mailed April 27, 2005. Upon entry of the amendments in this response, claims 1 – 9, 11, 12 and 28 remain pending. In particular, Applicant has amended claim 1, has added claim 28, and has canceled claims 10 and 13 - 27 without waiver, disclaimer or prejudice. Applicant has canceled claims 10 and 13 - 27 merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicant reserves the right to pursue the subject matter of these canceled claims in a continuing application, if Applicant so chooses, and does not intend to dedicate the canceled subject matter to the public. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections under 35 U.S.C. 102(e)

The Office Action indicates that claims 1-7, 9 and 11-12 are rejected under 35 U.S.C. 102(e) as being unpatentable by *Hsieh*. Applicant respectfully traverses the rejection.

With respect to *Hsieh*, *Hsieh* discloses:

> The etching of the polysilicon is accomplishes with a recipe comprising Cl_2 and HBr. ***The gate oxide layer(120)is also removed.***

(*Hsieh* column 4, lines 50-53 and FIGS. 2d). (Empasis added).

Additionally, *Hsieh* discloses:

> Then,the secomd nitride layer is etched to form nitride spacers(195) having a width and height between about 200 to 400 Å and 100 to 50 Å, respectively, as shown in FIG 2h.

(*Hsieh* column 5, lines 16-20 and FIGS. 2h-2j).

As shown in FIG.. 2d of *Hsieh*, since the gate oxide layer (120) is removed in the process of etching of the polysilicon(130), the gate oxide layer(120) is only exist under the floating gate(130). Thus, the nitride spacers(195) are formed on the substrate(100) not on the gate oxide layer, (*see* FIGs. 2h-2j).

In this regard, claim 1 recites:

> 1. A spilt gate flash memory cell structure comprising:
> a semiconductor region within a substrate extending to a surface;
> a gate insulator layer formed over said semiconductor surface;
> a conductive floating gate disposed over said gate insulator layer;
> a floating gate insulator layer disposed over said floating gate;
> ***sidewall insulator spacers disposed along bottom portions of sidewalls of said floating gate on said gate insulator layer***;
> an intergate insulator layer disposed over exposed portions of said gate insulator layer, said floating gate insulator layer and said sidewall insulator spacers; and
> a conductive control gate disposed over said intergate insulator layer and covering a portion of said floating gate.

(*Emphasis Added*).

Applicant respectfully asserts that the *Hsieh* is legally deficient for the purpose of anticipating claim 1. Specifically, Applicant respectfully asserts that *Hsieh* does not teach or otherwise disclose at least the features/limitation emphasized above in claim 1. Therefore, Applicant respectfully requests that the rejection of claim 1 be removed and that claim 1 be placed in condition for allowance.

Since claims 2 – 7, 9, 11 and 12 are dependent claims that incorporate the features/limitations of claim 1, Applicant respectfully asserts that these claims are in condition for allowance. Additionally, these claims recite other features/limitations that can serve as an independent basis for patentability.

Rejections under 35 U.S.C. 103(a)

The Office Action indicates that claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Hsieh*. As set forth above, Applicant has canceled claim 10 and respectfully asserts that the rejection as to this claim has been rendered moot. With respect to claim 8, Applicant respectfully traverses the rejection. In particular, Applicant respectfully asserts that claim 8 is a dependent claim that incorporates the features/limitations of claim 1, the allowability of which is discussed above. Therefore, Applicant respectfully asserts that claim 8 is in condition for allowance.

Newly Added Claims

Upon entry of the amendments in this response, Applicant has added new claim 28. Applicant respectfully asserts that this claim is in condition for allowance and that no new matter has been added.

With respect to claim 28, that claim recites:

> 28. A spilt gate flash memory cell structure comprising:
> a semiconductor region within a substrate extending to a surface;
> a gate insulator layer formed over said semiconductor surface;
> a conductive floating gate disposed over said gate insulator layer, ***the gate insulator layer extending outside of the conductive floating gate***;
> a floating gate insulator layer disposed over said floating gate;
> ***sidewall insulator spacers disposed along bottom portions of sidewalls of said floating gate adjacent said gate insulator layer***;
> an intergate insulator layer disposed over exposed portions of said gate insulator layer, said floating gate insulator layer and said sidewall insulator spacers; and
> a conductive control gate disposed over said intergate insulator layer and covering a portion of said floating gate.

(*Emphasis Added*).

Applicant respectfully asserts that the cited art is legally deficient for the purpose of rendering claim 28 unpatentable. Specifically, Applicant respectfully asserts that the cited art

does not teach or reasonably suggest at least the features/limitation emphasized above in claim 28. Therefore, Applicant respectfully requests that claim 28 be placed in condition for allowance.

Art Made of Record

The art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: _____
Daniel R. McClure, Reg. No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500